SPECIFICATION

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ION IMPLANTATION METHODS AND TRANSISTOR CELL LAYOUT FOR FIN TYPE TRANSISTORS

Background of Invention

[0001] This invention relates to the fabrication of a fin-type a metal oxide field effect transistor (MOS FET) integrated circuit (IC). In particular, it relates to placing the fins used to make fin-shaped MOS FET transistors on a substrate in a rectangular pattern of rows and columns and using adjacent fins as shields during irradiation with particles or light.

[0002] The continuing movement of integrated circuit technology toward smaller scales is making system level integration on a chip both possible and desirable. The conventional MOS transistor structure is a planer type in which current flows horizontally from source to drain. As transistor size shrinks to below about 0.1 μ m, the channel controlled by the gate also shrinks and unwanted couplings occur between the source and the drain, which is known as the "short channel problem." The short channel problem also increases power consumption and the difficulty of designing a properly functioning circuit.

[0003] A fin transistor (also known as a "pillar transistor") increases the size of the channel and reduces or eliminates the adverse effects of a short channel. Fin transistors can achieve a higher performance of current derivability because a fin transistor has a greater current flow area surrounding the gate or it uses a double gate. There are many inventions for fin-type MOSFET structures but because that structure is different from conventional planar transistors, new layout rules and manufacturing methods must be used when it is formed into an integrated circuit.

[0004] Referring to Figures 1a and 1b, fin-type MOS transistor 1 has substrate 2 that forms fin 3 having top 4 and two sidewalls 5. Over top 4 and sidewalls 5 of fin 3 is gate oxide 6 which is coated with conductive gate 7. Drain 8 and source 9 are on opposite sides of gate 7 at top 4 and sidewalls 5 of fin 3. (See also Figure. 2a of U.S. Patent No. 5,844,278.) Because there are current flow channels under gate oxide layer 6 at both top 4 and the two sidewalls 5 of fin 3, this structure has an increased channel area which increases current gain. Figures 1c and 1d show another kind of a fin-type MOS transistor. The transistor in Figures 1c and 1d has two channel areas on the sidewalls but does not have a channel area on the top of the fin. This structure is known as a dual gate or double gate transistor.

[0005] Figures 2a and 2b illustrate another fin-type MOS transistor structure known as a surrounded gate transistor (SGT) or a vertical transistor. (See Takato et al., "High Performance CMOS surrounding Gates Transistor (SGT) for Ultra High Density LSIs," pages 222-225, IEEE Electron Device Meeting (1988)). In Figures 2a and 2b, fin transistor 10 has substrate 11 which forms fin 12. Fin 12 is surrounded by gate oxide 13, which is covered by gate electrode 14. Drain 15 is at the top of fin 12 and source 16 covers substrate 11. Current flows through all four sidewall channels, which are controlled by surrounding gate electrode 14.

[0006] The fins can be fabricated on a bulk silicon substrate or on an SOI (silicon on insulator) deposited silicon layer. The fins are formed by selectively etching the substrate using RIE (reactive ion etching) techniques or by depositing amorphous silicon by a conventional CVD (chemical vapor deposition) technique.

[0007] Figures 3a to 3c show examples of conventional ion implantation processes for making planar silicon complementary metal oxide semiconductor (CMOS)large scale integrated circuits (LSI). In Figure 3a, N-type silicon substrate 17 has been coated with photoresist layer 18, which has been exposed to light and etched away at 19. Ion implantation with boron from the direction shown by the arrows creates P-type well 20. In Figure 3b, substrate 21 of N-type silicon has been coated with a photoresist 22 which has been developed and etched away elsewhere. Gate oxide 23 and gate electrode 24 have been deposited and boron ion implantation from the direction of the arrows has formed a P-type diffusion layer 25. The resulting P-channel transistor

has source 26 and drain 27.

[0008] In Figure 3c, boron ion implantation was used to create P-type well 28 in an N-type silicon substrate 29 and phosphorus or arsenic ion implantation formed source 30 and drain 31.

Summary of Invention

[0009] An object of the present invention is to provide high performance, area-efficient fin-type MOS FET manufacturing methods, without the need for special processes, and to reduce the need for masking processes such as ion implantation.

[0010] Another object of the invention is to provide high performance, area-efficient fin-type MOS FET layout methods for large scale integrated circuits (LSI).

[0011] MOS FET ICs made according to the method of this invention have an ultra-high integration density and a higher performance for short channels and low operation voltages than ICs made with conventional planar type MOS FET transistors.

Brief Description of Drawings

[0012] Figure 1a is an isometric view showing the structure of a fin-type transistor.

[0013] Figure 1b is a cross-sectional view through B-B in Figure 1a.

[0014] Figure 1c is an isometric view showing the structure of a dual gate transistor.

[0015] Figure 1d is a cross-sectional view through B-B in Figure 1c.

[0016] Figure 2a is an isometric view showing the structure of another fin-type transistor.

[0017] Figure 2b is a cross-sectional view through B-B in Figure 2a.

[0018] Figures 3a to 3c are front views in section illustrating ion implantation process steps for making a conventional planar CMOS LSI.

[0019] Figure 4 is a front view in section showing a certain presently preferred embodiment of the process of this invention, illustrating the maximum angle of ion implantation and minimum distance between transistors in adjacent rows.

[0020] Figure 5 is a plan view showing two groups of transistors laid out in a square pattern.

[0021] Figure 6 is an isometric view in section illustrating a process of this invention for fabricating N-type and P-type transistors on the same fin.

[0022] Figure 7 is an isometric view in section showing the structure formed from the process illustrated in Figure 6.

[0023] Figure 8 is a side view in section illustrating another process of this invention, where a photoresist is used.

[0024] Figure 9 is a side view in section showing the results of the process illustrated in Figure 8.

[0025] Figure 10 is a side view in section illustrating the use of a mask patterning step in the process of this of invention.

[0026] Figure 11 is a side view in section showing contact holes formed from the process illustrated in Figure 10.

[0027] Figure 12 is an isometric view illustrating the application of a metal layer to the structure shown in Figure 11.

[0028] Figure 13 is a diagram illustrating a conventional inverter circuit for a transistor.

[0029] Figure 14 is a plan view showing an embodiment of the circuit of Figure 13 using the structure of Figure 7.

[0030] Figure 15 is an isometric view showing an alternative embodiment of this invention, where the fin transistors have a common source terminal.

[0031] Figure 16 is a plan view showing an example of an inverter circuit that uses the structure shown in Figure 15.

[0032] Figure 17 is a plan view showing a checkerboard pattern of transistors on a substrate.

[0033] Figure 18 is an isometric view showing an alternative embodiment of this

invention, where the fin transistors have a common source terminal with multi fins.

Detailed Description

[0034] It will be understood from this description that the present invention can be implemented in conventional MOSFET technology, and that the described embodiments will operate accordingly if designed and fabricated in accordance with known complementary metal oxide semiconductor (CMOS) and silicon on insulator (SOI) rules and methodologies. These rules and methodologies are well-known in the art and will not be repeated for this description. SOI materials meeting this criterion are well-known in the art. In this invention, the term "fin transistor" includes both the structures of Figures 1a, 1b, 1c, 1d, 2a, and 2b, as well as related structures where the channels are on 2, 3, or 4 sides, and the embodiments shown in the other drawings are applicable to any of these structures unless otherwise noted.

[0035] In this invention, the fins of fin transistors are arranged in rectangular patterns of rows and columns. The fins can occupy each square in a grid of rows and columns, as in Figure 5, which will be called a "square pattern," Alternatively, the fins can occupy every other position in each row and column, where each row is offset by one fin from the adjacent row, which will be called a "checkerboard pattern," as shown in Figure 17. The checkerboard pattern permits a higher packing of the transistors, but the square pattern is more suitable for other purposes, such as when the fins are elongated and more than one transistor is fabricated on each fin. Other patterns and combinations of square and checkerboard patterns can also be used, as long as the fins are positioned to shield the substrate in between them during angled radiation.

[0036] Referring to Figure 4, the sidewalls of the fins are implanted at an angle θ . The angle θ and the distance D between the rows are selected so that the fins in one row shield the substrate in between the fins from the radiation, yet permit the radiation to impinge upon the sidewalls of the fins in the adjacent row. In effect, the shadows of the fins in one row fall at the base of the fins in the next row. If an SGT transistor is to be fabricated, the fins in the rows can shield the substrate for one angled radiation exposure, then the fins in the columns can shield the substrate for a second angled radiation exposure at 90 degrees to the first exposure. The above-described angled and multi-directional ion implantations can be achieved by providing a wafer holder

[redacted]

that can be rotated 360 degrees holding wafers at an angle of 0 to 75 degrees to the ion beam direction.

[0037] Figure 4 shows an embodiment of the present invention where the ion implantation is multi-directional. In Figure 4, fins 32 have been fabricated on substrate 33. Each fin 32 has a top 34 with diffused layer 35 and two sidewalls 36 coated with gate oxide 37 and then with gate electrode material 38. Top 34 is implanted in a vertical direction. Fins 32 have been positioned on substrate 33 at a distance D apart. Angle θ , at which sidewalls 36 are implanted, is selected so that top 34 of a fin in one row shields substrate 33 between that fin and the fin in the next row. That is, the ion beam impinges on sidewall 36, but does not impinge on substrate 33. By implanting from each side, both sidewalls 36 can be implanted.

[0038] The minimum sidewall layout distance D, the sidewall height H, and the angle θ of ion beam from vertical are related according to the equation $D \approx H \tan \theta$, where " $\approx$ " means "is approximately equal to." Using this equation, the sidewall surfaces can be implanted in a single ion implantation step without using a mask or a special process to protect the substrate because the fins themselves act as a mask to prevent implantation of the substrate. If the substrate is not shielded, it may be implanted, which will adversely affect its stability because a channel may be formed in between the fins. The distance D is the distance needed to shield the substrate, yet permit implantation of the sidewalls of the fins in the adjacent row. The distance D need not be 100% precise, as some implantation of the substrate or failure to implant the bottom of the sidewall of the adjacent fin will not result in a failure of the resulting transistor to function properly. For a 2-sided channel (e.g., Figure 1a), the distance between the columns need not be equal to the distance D between the rows as implantation does not occur in that direction and shielding is not needed; therefore, the distance between columns can be substantially more or less than the distance D. For 4-sided channels (SGT, e.g., Figure 2a), the distance between the columns is preferably the same as the distance D between the rows. To implant the sidewalls of fins on the edge of the chip, dummy fins can be fabricated that are not made into transistors or are not connected into the circuit.

[0039]

The fins (sometimes also referred to as "pillars") are rectangular solids (i.e., each

side and the top is a rectangle), but they need not be cubes or have square sides or a square top. Typically, the pillars will be about 0.03 to about 0.13 μ m high and will be about 0.03 to about 0.13 μ m apart (the distance D). The angle θ is typically about 30 to about 75 degrees.

[0040] Because the top transistor channel is implanted twice, once when the left sidewall is implanted and once when the right sidewall is implanted, the opposite type of ion can be implanted only on the top surface using a vertical beam, which compensates for the double dose on the top from the two angled implantations.

[0041] Figure 5 shows another embodiment of the invention. In this embodiment, fin transistors 38 are arranged in a square pattern on a grid of rows and columns on substrate 39. In the ion beam directions of I and II, both sidewalls 40 of the fin transistors of Group A are implanted, but the sidewalls 41 of the fin transistors in Group B are not implanted. On the other hand, in the ion beam direction of III or IV, both sidewalls 41 of the fin transistors in Group B are implanted but the sidewalls 40 of the fin transistors in Group A are not implanted. In both cases, the distance D is the minimum distance needed for a particular angle θ . By turning the transistors 90 degrees in alternating rows, as shown in Figure 5, the process of this invention can be used to produce fin transistors on the same substrate that have different threshold voltages.

[0042] Figures 6 and 7 illustrate forming both N and P-type transistors on the same fin. Fin 42 is formed on N-type substrate 43. A portion of the substrate and fin has been protected with photoresist 44 and the remaining portion 45 has been ion implanted with boron from the directions shown to make P-type well 46 in substrate 43. N-type transistor 47 and P-type transistor 48 have been fabricated over fin 42 after removal of photoresist 44, as shown in Figure 7, thereby producing a CMOS transistor. (U.S. Patent Nos. 6,255,699 and 6,413,802 also disclose CMOS transistors formed on the same fin. U.S. Patent No. 6,255,699 shows a P-channel and an N-channel transistor for each sidewall, and the U.S. Patent No. 6,413,802 shows a stacked fin structure of P-and N-channel transistors. However, both of those inventions require extra process steps.) In Figure 8, an angled light beam irradiates and develops positive photoresist 49, which covers fins 50 on substrate 51. Figure 9 shows the results after the exposed

pohotoresist has been removed. (If a negative photoresist is used in Figure 8, it would remain on the top and left sidewalls.) In Figure 9, top 52 can now be separately implanted using an ion beam coming from any direction so that top 52 and the right and left sidewalls can have different threshold voltages without the need for a mask.

[0043] In Figures 10 and 11, fins 53 on substrate 54 have been covered with positive photoresist 55. Light or ions pass through mask 56 to form a pattern 57 on sidewalls 58 of fin 53, as shown in Figure 11. One embodiment of this pattern on the sidewalls can be contact holes 57. Contact holes 57 through insulator 60 allow electrical access to the drain and source regions. They can be connected with a metal layer 59 over insulator layer 60, as shown in Figure 12. Because contact holes 57 are on sidewalls 58 instead of on substrate 54, the transistors can be closer together. This sidewall patterning method is also applicable to MEMS (micro electromechanical systems).

[0044] Figure 14 illustrates an inverter circuit as shown in Figure 13 and one embodiment of Figure 7.

[0045] In Figure 15, transistors 61 are constructed on a single fin 62 of substrate 63, where source terminal 64 is common and drain terminals 65 are in both directions. By using the common source terminal as shown in Figure 15, an inverter circuit as shown in Figure 13 can be made that covers a very small area, giving a structure such as that shown in Figure 16. (Each area enclosed by dotted lines in Figure 16 contains two of the structures shown in Figure 15.) This common source fin structure can be extended to multi-fin structures, as shown in Figure 18. (Common gate multi-fin structures are disclosed in Figure 6 of U.S. Patent No. 6,413,802.) Figure 17 is similar to Figure 5, but shows transistors 63 in a checkerboard pattern. In Figure 17, the distance between the rows (D) is not the same as the distance between the columns (d).

[0046] While the invention has been particularly shown and described with reference to a preferred embodiment or, not, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.